Crosstalk Suppression in a 650-V GaN FET Bridge-leg Converter using 6.7-GHz Active Gate Driver

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Abstract— **With switching transients as fast as 100 V/ns and a low threshold voltage of 1-2 V, GaN FETs in bridge-leg topologies are potentially vulnerable to crosstalk and the resultant unwanted partial turn-on, noise interference, and increased losses. Constant-strength gate drivers for GaN FETs limit switching speed to suppress crosstalk. In this work, active gate driving is shown to permit faster switching, whilst still suppressing crosstalk. This is demonstrated in a GaN FET bridge-leg converter. The control device transients are shaped to reduce crosstalk, whilst the synchronous device's gate impedance is actively varied to increase its immunity to crosstalk. This is carried out using two 6.7-GHz active gate drivers that can dynamically vary their output resistance from 0.12 Ω to 64 Ω every 150 ps during the sub-10-ns switching transients. It is demonstrated that unwanted turn-on is suppressed without incurring undershoot and oscillation in the gate, that negative spurious gate voltages can be greatly reduced, and that oscillations in the transient drain current are damped, without incurring additional loss.**

Keywords— Gallium Nitride (GaN); active gate driver; variable gate resistance; crosstalk; spurious turn-on; oscillation; bridge-leg

I. INTRODUCTION

Transient currents or voltages generate electro-magnetic fields; any conductor in the circuit that interacts with this field through capacitive, inductive or conductive coupling has crosstalk noise imposed on it [1]. Crosstalk is a crucial cause of excessive power losses and EMI in fast-switching power converters [2]-[10]. As illustrated in Fig. 1, the turn-on of the high-side control device generates a displacement current through the gate-drain capacitance of the low-side synchronous device, charging up its gate-source capacitance and leading to an unwanted positive spurious gate voltage in the synchronous device. This voltage, if exceeding the threshold voltage of the power device, would induce cross-conduction and consequently more switching losses and even shoot-through [2]-[8]. Likewise, a negative spurious gate voltage is generated in the synchronous device at the turn-off of the control device. The faster switching transients of GaN FETs, along with their relatively low threshold voltages, increase the likelihood of crosstalk causing excessive cross-conduction losses, noise interference, and instability [6]-[7]. Besides, a negative gate-source voltage increases the reverse conduction voltage of GaN FETs, thus increasing loss during the dead time [11].

These crosstalk-induced problems can be individually addressed by various methods in Si/SiC MOSFETs and Si IGBTs. However, slowing down the switching speed to reduce noise interference and spurious gate voltages increases switching losses [8]. A BJT/MOSFET or additional external gate-source capacitance in parallel with the gate would increase the gate input capacitance and hence switching losses, more importantly, even a small amount of parasitic inductance between the external component and the GaN gate may cause high-frequency oscillations and exacerbate the problem [8] [11]. A minimal gate resistance is often recommended for a low-impedance pull-down at turn-off, however, it leads to gate undershoot and high-frequency oscillations in GaN FETs, which implies higher dead-time conduction loss [11]. Moreover, as will be shown later, crosstalk is still likely to be significant at fast switching transients even with a minimal turn-off gate resistance [7]. A negative off-state gate voltage can bring the positive spurious gate voltage below threshold voltage [3]-[5], however this increases the dead-time conduction loss of GaN FETs, and together with the negative spurious gate voltage, may degrade the reliability of the synchronous device through exceeding the maximum allowable negative gate voltage [12]. In short, these methods mitigate only a sub-set of the crosstalk-induced problems, and they have limitations in GaN FETs. They also only either address problems associated with the synchronous device, or with the control device.

In this paper, a fully-active approach is adopted, where gate drivers on both devices in a bridge-leg act in unison to avoid crosstalk, as illustrated in Fig. 2. The control device is actively controlled to create less crosstalk on both transients, whilst the synchronous device's gate impedance is adjusted to make it more immune to interference. This is done by driving each GaN FET with a 6.7-GHz integrated active gate driver [13], which has been previously demonstrated to allow the shaping of the switching waveforms of 40-V [13]-[14] and 650-V GaN FETs [15] in a bridge-leg converter for overshoot, oscillation and EMI reduction. The driver can be programmed to vary its output resistance from 0.12 Ω to 64 Ω every 150 ps.

This digest is organised as follows: Section II presents test setup and the active gate driver; Section III demonstrates experimental results for crosstalk suppression in a fast-switched GaN bridge-leg through the simultaneous active driving of both devices; Section IV draws conclusions.

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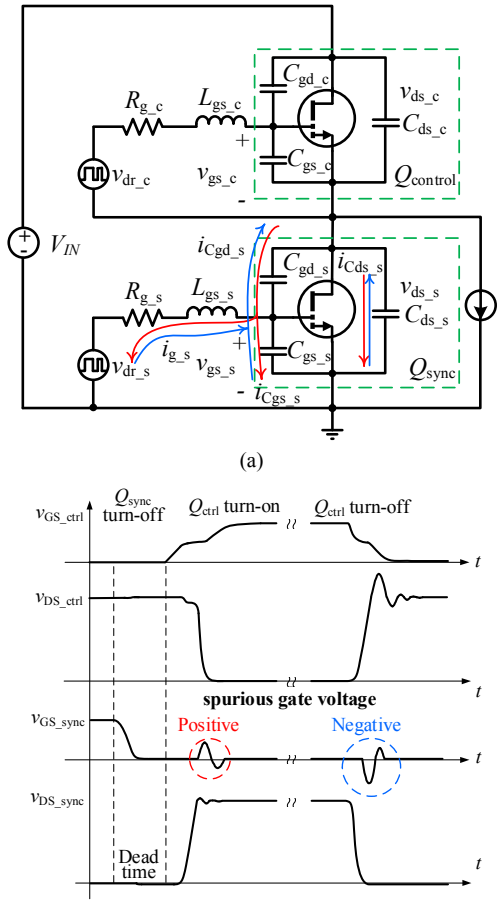

Fig. 1. An example of crosstalk mechanism in a bridge-leg converter. (a) Displacement currents through the low-side synchronous device during switching of the high-side control device. (b) Impact on the gate-source voltage of the synchronous device.

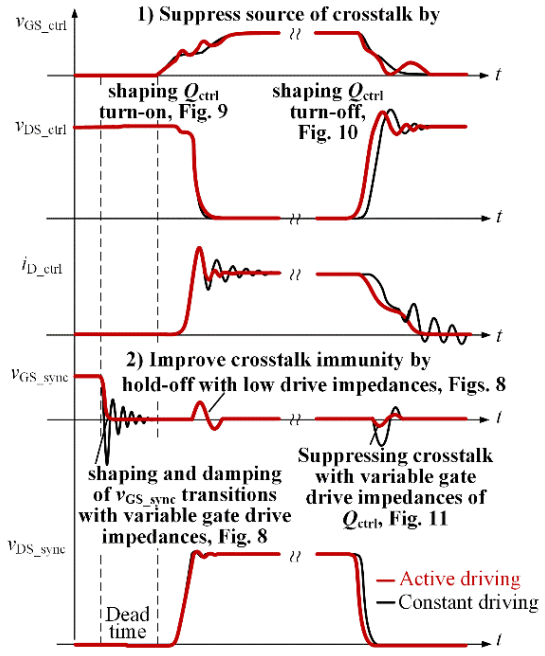

Fig. 2. Gate driving strategy, examined here, to avoid crosstalk by actively driving both devices in the bridge-leg.

II. Test Setup and 6.7-GHz Active Gate Driver

The test circuit is shown in Fig. 3, configured for a negative (a), or positive (b) load current. The circuit is operated in double-pulse mode. Each GaN device is driven by a 6.7-GHz active gate driver. The DC link voltage V_{IN} is 300 V. The control device is turned on for 2.93 µs to establish an output current of 10 A in the 88-µH output inductor. Fig. 4 shows the power board containing two GS66508P 650-V GaN FETs and their respective active gate drivers.

As illustrated in Fig. 5, the 6.7-GHz active gate driver consists of high-speed programmable memory that holds the gate drive sequences, logic circuit that controls output stage during switching transients, and impedance-adjustable output stage that allows simultaneous operation of parallel pull-up and pull-down. During switching transients, the gate driver can activate a near-arbitrary sequence of pull-up or pull-down output resistances between 0.12 Ω and 64 Ω. A hybrid of clocked and asynchronous control logic with 150-ps delay elements achieves an effective resistance update rate of 6.7 GHz during switching events. Details of the driver architecture are provided in [13]. The output of the driver can be set to a constant gate strength to compare with the results of active gate driving, although the effective gate resistance is then voltage dependent [13].

The configuration of the experimental hardware is illustrated in Fig. 6. A Diligent Zedboard with a Xilinx Zync 7000 series system-on-chip (SoC) provides a user interface to configure the gate drivers and program them. Prior to testing, the host computer sends the desired drive sequences to the Xilinx system, which in turn programs the gate drivers. A Keysight 81150A function generator, which is configured with the desired double-pulse gate-driver control signals from MATLAB, has its output passed into and through the Xilinx system to the gate drivers.

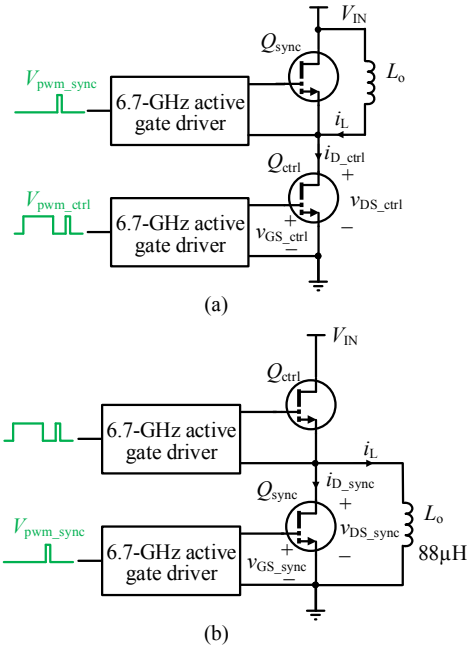

Fig. 3. Bridge-leg converter using active gate drivers for both GaN devices. (a) Configuration for control-device measurement in Figs. 7, 9 and 10. (b) Configuration for synchronous-device measurement in Figs. 8 and 11.

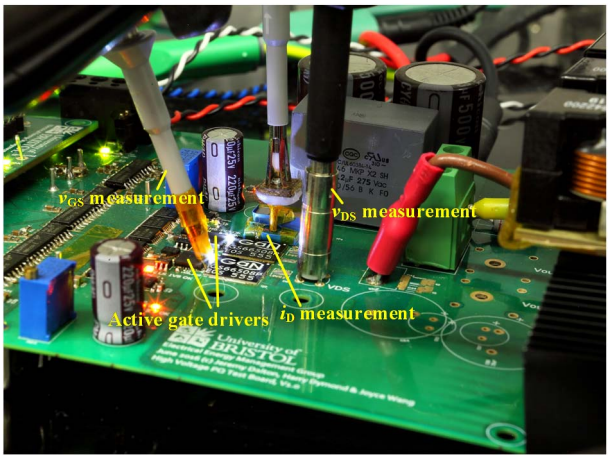

Fig. 4. Detailed view of the power board.

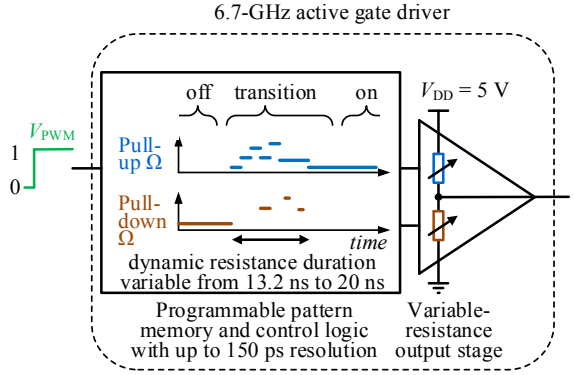

Fig. 5. Concept of the active gate driver used to control GaN FETs.

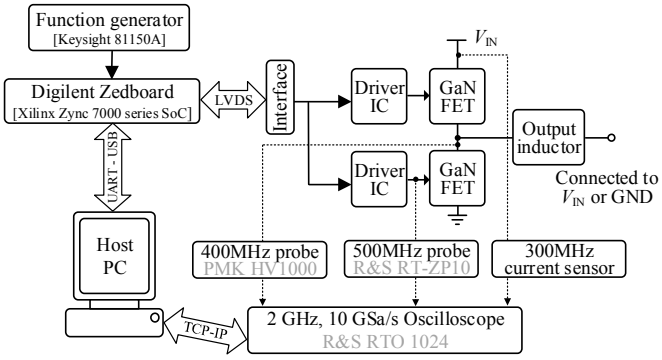

Fig. 6. Test setup with driver programming and waveform measurement.

Switching waveforms are captured and de-skewed on a Rhode & Schwarz RTO1024 2-GHz 10-GSa/s oscilloscope. The double pulse test circuit of Fig. 3 (a) is used for waveform measurements on the control device in Figs. 7, 9 and 10, and that of Fig. 3 (b) on the synchronous device in Figs. 8 and 11, to permit high-bandwidth ground-referenced measurement, as wideband floating high-voltage measurement is problematic. Each capture of switching waveforms is repeated ten times and averaged by carrying out a train of ten double-pulse tests. As shown in Fig. 4, the gate-source voltage v_{GS} is measured by R&S RT-ZP10 10:1 500-MHz with spring tips directly probing at the gate and source terminals of the GaN device; the drain-source voltage v_{DS} is measured by PMK HV1000 100:1 400-MHz passive voltage probe connecting through a probe adapter to the drain and source terminals. Such minimum loop-inductance connections are essential for making high-bandwidth measurements. The drain current i_D is measured by a custom non-invasive and floating current sensor with a 0.2 nH increase in the power loop inductance and a bandwidth of 300 MHz. Low insertion inductance is important so that it exerts the least influence on the inductance-sensitive GaN switching transient. This current sensor can also be used to measure the current of the low-side device.

III. Experimental Results

A. *Improving crosstalk immunity of the synchronous device during control-device turn-on*

The impact of the synchronous-device gate resistance R_{G_sync} on the control-device turn-on is illustrated in Fig. 7. The turn-on gate resistance of the control device R_{G_ctrl} is 9 Ω for all three scenarios. The turn-on switching loss of the control device for each scenario is estimated using the same method as described in [15], and is provided in the line labels in the drain current i_{D_ctrl} graph. With the increase in R_{G_sync}, the positive spurious gate voltage in the synchronous device is higher [3]-[4]; the synchronous device that is supposed to be off is partially turned on, resulting in more i_{D_ctrl}, slower slew rate of the drain-source voltage v_{DS_ctrl}, and more switching loss. It shows that gate driving of the synchronous device can influence the control-device turn-on, and a minimum R_{G_sync} is desired to suppress crosstalk and avoid cross conduction at this transient. However, a minimum R_{G_sync} often incurs gate undershoot and oscillation at the turn-off edge of the synchronous device.

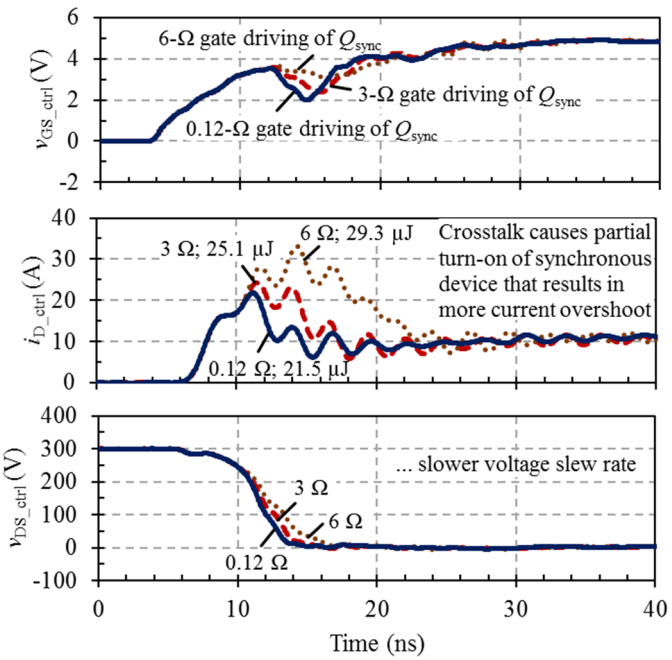

Fig. 7. Turn-on switching waveforms of the control device when the synchronous devices is held off with 0.12-Ω, 3-Ω, and 6-Ω gate resistance respectively. R_{G_ctrl} is 9 Ω in all three scenarios.

Fig. 8 shows the measured switching waveforms of the synchronous device during synchronous-device turn-off and control-device turn-on for 0.12-Ω and 4.7-Ω fixed gate resistance driving, and active gate driving of the synchronous device. The turn-on R_{G_ctrl} is 9 Ω in all three scenarios. 0.12 Ω provides the strongest pull-down to generate the minimum positive spurious gate voltage. However, as shown in the dashed waveform of Fig. 8, it incurs oscillation and undershoot in the gate-source voltage of the synchronous device v_{GS_sync}, which would increase the dead-time conduction loss and oscillation [8], [11]-[12]. As shown in the dotted waveform of Fig. 8, 4.7 Ω is the minimum R_{G_sync} to avoid undershoot and oscillation in v_{GS_sync}, however the turn-off switching time is longer, and the positive spurious gate voltage exceeds the threshold voltage of around 1.4 V [16].

The active gate driving strategy is shown at the bottom of Fig. 8. A strong pull-down is applied at the beginning of the synchronous-device turn-off to speed up the initial transient; the pull-down strength is gradually reduced by either increasing the pull-down resistance or adding a momentary pull-up so that v_{GS_sync} falls fast enough but without undershoot and oscillations; the GaN gate is pulled down with the strongest driving strength at the end of the turn-off transient to enhance crosstalk immunity. The result of active gate driving of the synchronous device is a v_{GS_sync} without undershoot and oscillation and with minimum positive spurious voltage, i.e. crosstalk. It breaks the link between crosstalk immunity and gate undershoot and oscillation.

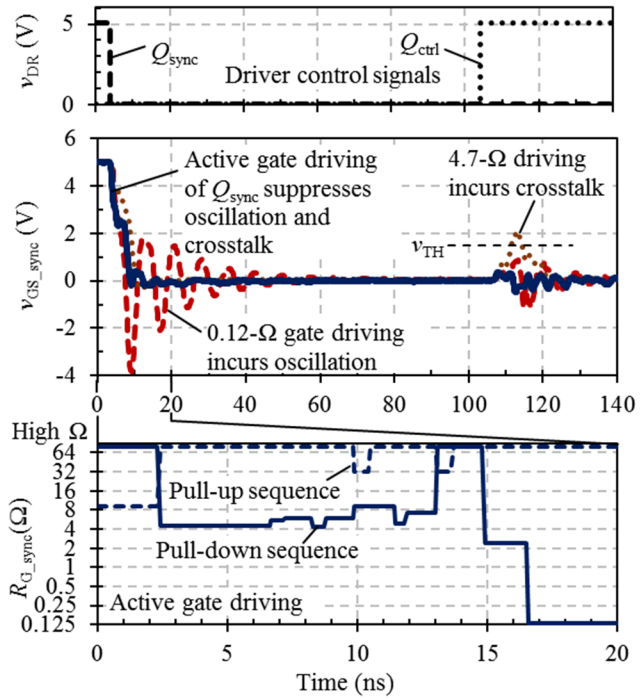

Fig. 8. Switching waveforms of the synchronous device using 0.12-Ω, 4.7-Ω constant gate driving, and active gate driving of the synchronous device. Turn-off of synchronous device at 2.5 ns, and turn-on of control device at 102.5 ns. R_{G_ctrl} is 9 Ω for all three scenarios.

B. Reducing cause of crosstalk at turn-on without a reduction in switching speed

Fig. 9 shows the measured turn-on switching waveforms of the control device for 7.2-Ω, 18-Ω constant gate driving and active gate driving of the control device. R_{G_sync} during the same switching transient is 0.12 Ω for all three scenarios. The turn-on switching loss of the control device for each scenario is provided in the line labels in the i_{D_ctrl} graph. Current oscillation is observed at the capacitive discharge phase where v_{DS_ctrl} falls and i_{D_ctrl} overshoots. It is demonstrated that compared to 7.2-Ω driving, 18-Ω driving reduces current overshoot by 23%, damps but still does not eliminate the oscillation in the drain current, moreover, the switching time and switching loss are increased by 67% and 29% respectively.

In order to maintain the switching time and loss whilst damping the current oscillation, the active gate resistance sequence as shown at the top of Fig. 9 speeds up the turn-on delay time before i_{D_ctrl} rises, gradually decreases the gate drive strength during current rise time to limit the drain current slew rate, increases the drive strength afterwards to reduce the voltage fall time, temporarily decreases the drive strength to reduce the oscillation after the fall in v_{DS_ctrl} is about to finish, and pulls up the device with a strong driving strength at the end. In contrast to results with constant gate driving, the active resistance sequence of Fig. 9 eliminates the oscillation in the drain current with only 2% increase in switching loss and no change in the overall switching time. Active gate driving can thereby achieve a much better trade-off between switching loss and drain current oscillation that is a potential cause of crosstalk.

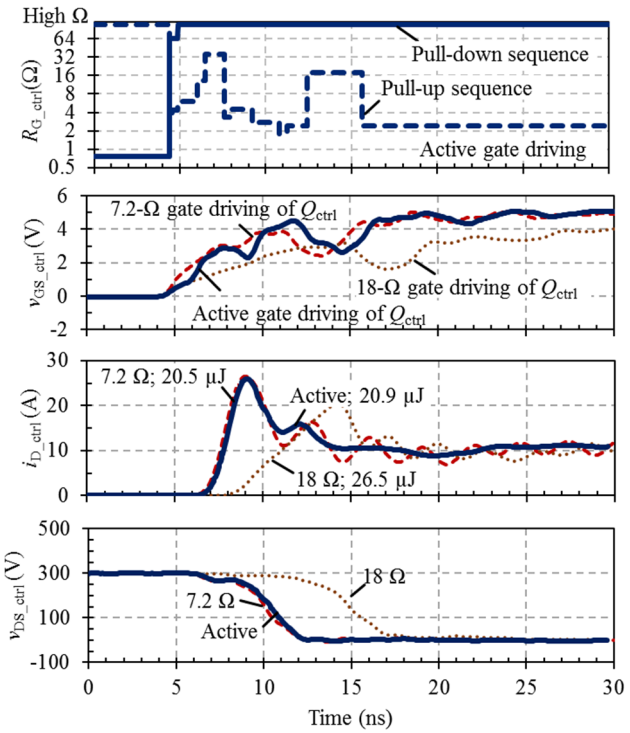

Fig. 9. Reduction in a potential cause of crosstalk at turn-on. Three switching strategies for control device: 7.2-Ω, 18-Ω, and active gate driving. R_{G_sync} during this transient is 0.12 Ω for all three scenarios.

C. *Reducing cause of crosstalk at turn-off without a reduction in switching speed*

Fig. 10 shows the measured turn-off switching waveforms of the control device for 9-Ω, 18-Ω constant gate driving and active gate driving of the control device. R_{G_sync} during the same switching transient is 0.12 Ω for all three scenarios. The turn-off switching loss of the control device for each scenario is estimated using the same method as described in [15], and is provided in the line labels in the i_{D_ctrl} graph. 9-Ω constant gate driving shows oscillation in i_{D_ctrl}. v_{GS_ctrl} has dropped below the gate threshold voltage, turning the channel off, before v_{DS_ctrl} rises to its off-state value. Therefore, the gate driver is not in full control of the device transients. These are instead set by the output current charging the GaN devices' voltage-dependent output capacitances. The oscillation is not reduced by increasing R_{G_ctrl} to 18 Ω, for the gate driver has lost control of the commutation as in 9-Ω driving. It is only possible for the gate driving to influence the current oscillation if it resumes control of the switching. In order to reactivate the control at the end of the transient, the active gate drive sequence shown at the top of Fig. 10 temporarily disables pull-down and enables three short pull-ups, that is, in opposition to the polarity indicated by the PWM signal. This is seen to reverse the gradient of v_{GS_ctrl} and dramatically reduce the oscillation in i_{D_ctrl}. The early phase of the commutation is accelerated to reduce the switching time and overlap loss. The active gate driving is seen to reduce current oscillation at turn-off transient that is a potential cause of crosstalk whilst maintaining the switching loss.

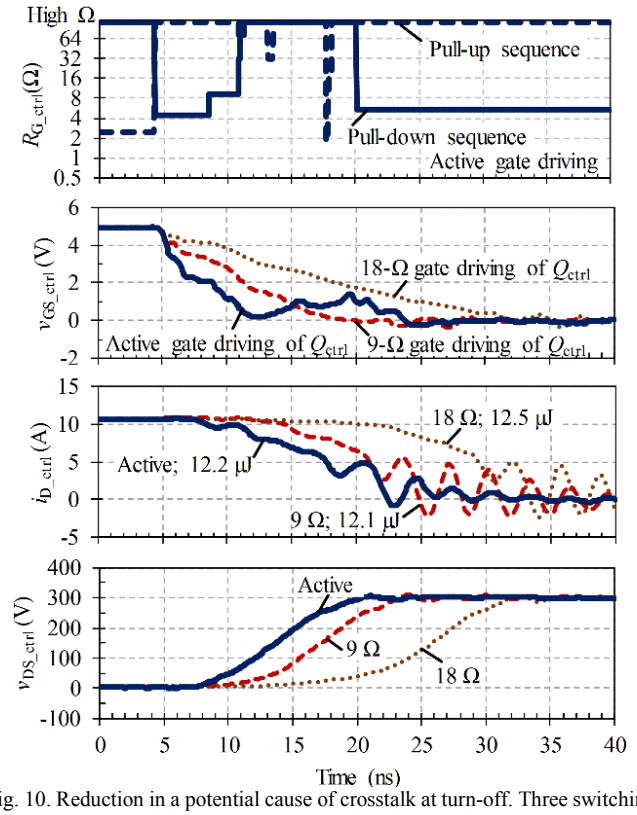

Fig. 10. Reduction in a potential cause of crosstalk at turn-off. Three switching strategies for control device: 9-Ω, 18-Ω, and active gate driving. R_{G_sync} during this transient is 0.12 Ω for all three scenarios.

D. *Crosstalk suppression at control-device turn-off*

Fig. 11 shows the measured switching waveforms of the synchronous device at control-device turn-off for 4.5-Ω, 18-Ω constant gate driving and active gate driving of the control device. R_{G_sync} during the same transient is 0.12 Ω for all three scenarios, however, as the two constant gate driving scenarios demonstrate, there is still significant negative spurious gate voltage and oscillation, that is, the minimum pull-down R_{G_sync} still fails to limit unwanted crosstalk at this transient. Increasing R_{G_ctrl} to 18 Ω does not help either, for the gate driver has lost control of the device voltage transients as shown in Fig. 10.

The active gate drive sequence at the top of Fig. 11 temporarily disables pull-down and enables four short pull-ups to regain the gate control and slow down v_{DS_sync} when the spurious gate voltage is induced. Thereby, active gate driving of the control device manages to maintain the fast slew rate of v_{DS_sync}, reduce the negative spurious gate voltage by 64% and eliminate the oscillation in the gate and the drain current afterwards. Besides, the 4.5-Ω transition in the v_{DS_sync} waveform starts smoothly but has an abrupt end; the active gate driving rounds off the corner, which would reduce the high-frequency spectral content of v_{DS_sync} [17]. These would not be possible with constant gate driving even by sacrificing switching speed.

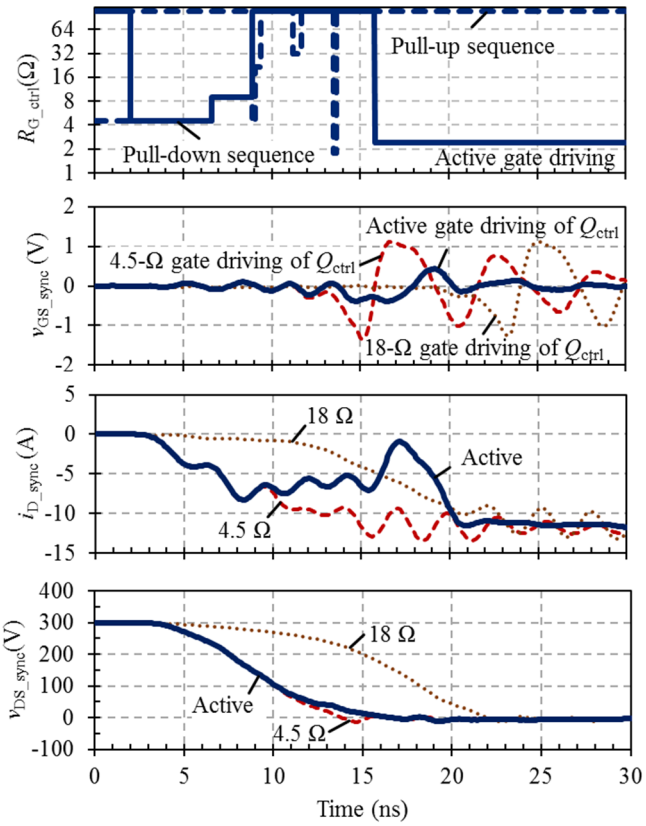

Fig. 11. Synchronous device waveforms resulting from reducing crosstalk at control device turn-off, for three control-device gate driving scenarios: 4.5-Ω, 18-Ω, and active gate driving. R_{G_sync} during this transient is 0.12 Ω for all three scenarios.

IV. Conclusions

Active gate driving has been demonstrated to suppress crosstalk and therefore facilitate the fast switching of GaN FETs at 100 V/ns. Experimental results of a bridge-leg converter show that, active gate driving of the synchronous device permits having a strong pull-down to minimise instances of positive spurious gate voltage at control-device turn-on, whilst eliminating gate undershoot and oscillation with variable gate drive impedances at synchronous-device turn-off. Active driving of both turn-on and turn-off transients of the control device reduces oscillation in the drain current with almost no increase in switching loss. At control-device turn-off, crosstalk is still significant, even when using a low turn-off gate resistance for the synchronous device. At this point, the control device's gate is normally no longer in control of the switching transient. Active gate driving is shown to bring the switching back under control by temporarily bringing the gate voltage back to the threshold voltage. In this way, it is possible to supress negative spurious gate voltages, and reduce oscillation and high-frequency content of the switching waveforms. In conclusion, active gate driving that allows the gate impedance to be varied at a resolution of 150 ps could potentially provide a solution to crosstalk in GaN-based converters.

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